**RUTHVIK REDDY ANTHIREDDIGARI**

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**SUMMARY**

I am a graduate with a strong foundation in digital design and FPGA development seeking an entry level role at your organization. With experience in Verilog and C for circuit design and implementation, I can develop and optimize circuits for performance, generate timing diagrams and smooth collaboration with others to complete projects.

**EDUCATION**

**Manipal Institute of Technology, MAHE, Manipal** Oct 2020 - July 2024

**Bachelors in Technology,** Major in Electrical and Electronics Engineering.

**Relevant coursework** : Basic Electronics, Analog System Design & LAB, Digital System Design & LAB, FPGA Design.

**SKILLS**

* **Languages**: Verilog, VHDL, Arduino, C.
* **Tools**: LT SPICE, MATLAB/SIMULINK, PROTEUS, LABVIEW, Kiel uvision, KI-CAD.
* **RTL design tools**: Questa Sim/Model Sim, Xilinx Vivado, and Xilinx Vitis.
* **Hardware:** Altera Max V/10, Xilinx Zynq 7000, Artix-7, Arduino Uno, 8051 uc, Analog and Digital ICs.

**INTERNSHIP EXPERIENCE**

**Delta IOT Solutions Private limited, Hyderabad, India Mar 2025 – Present**

***Intern – Embedded***

* **Developed and implemented Embedded C code for Arduino and ESP32-based IoT projects.**
* **Assisted in designing custom PCBs based on existing schematics, supporting prototyping and hardware development.**
* **Helped in hardware testing, troubleshooting, and circuit board development, contributing to debugging processes.**

**Research Centre Imarat, DRDO , Hyderabad, India** Feb 2024 – June 2024

*Student/Project Intern*

* Engineered a low-latency, power-efficient video data streaming system using AXI4-Stream and AMBA protocols, reducing latency by 15% and power consumption by 10%.
* Designed and verified RTL using VHDL/Verilog and C programs for high-speed and reliable data transfer on Xilinx FPGAs.
* Utilized Vivado and Vitis toolchains for synthesis, implementation, and testing, alongside reliability and timing validation to ensure design robustness.

**Boeing India Private Limited , Bengaluru , India** Jun 2023 – Aug 2023

*Electrical Design and Analysis Engineer Intern.*

* Developed and optimized UART interface with FIFO buffers using FSMs in Verilog, enabling reliable communication for FPGA-based systems.
* Used Intel Quartus and ModelSim for simulation, debugging, and verification, achieving timing and functional correctness.
* Contributed to a 15% reduction in design size and a 20–25% cost savings through logic optimization and efficient FPGA resource utilization.

**ACADEMIC RESEARCH**

*Rectifier based buck converter prototype for charging* applications ([Link](https://github.com/Ruthvik-reddy-A/Rectifier-based-buck-converter-prototype-for-charging-applications)) Aug 2022 – May 2023

* Developed a high-efficiency DC-DC buck converter, using MOSFET- and diode-based switching mechanism improving charging efficiency by 10% and reducing voltage fluctuations, crucial for power management in circuits.
* Simulated and optimized circuit performance in LTspice and Simulink, achieving a 15% reduction in power loss, reinforcing expertise in power design and hardware modeling as well as a compact, low-cost module.

**CERTIFICATIONS**

* Introduction to FPGA Design for Embedded Systems, Coursera – University of Colorado Boulder.([Link](https://github.com/Ruthvik-reddy-A/CERTIFICATES/blob/master/Coursera%20fpga1.pdf))
* Hardware Description Languages for FPGA Design, Coursera – University of Colorado, Boulder ([Link](https://github.com/Ruthvik-reddy-A/CERTIFICATES/blob/master/Coursera%20fpga2.pdf))
* VLSI Design Flow : RTL to GDS, NPTEL – IIIT, Delhi ([Link](https://github.com/Ruthvik-reddy-A/CERTIFICATES/blob/master/VLSI%20Design%20Flow_%20RTL%20to%20GDS.pdf))
* Semiconductor Fabrication 101 – Purdue University, UT Austin, Intel Corporation